APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: GENERATING PULSES FOR RESETTING INTEGRATED CIRCUITS

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GENERATING PULSES FOR RESETTING INTEGRATED CIRCUITS

Background

This invention relates generally to integrated circuits and particularly to systems for starting up integrated circuits.

During the start-up cycle of an integrated circuit, the supply voltage ramps up. A power-on reset circuit generally asserts reset whenever the supply voltage falls below a threshold. Moreover, the reset circuit asserts a reset until the supply voltage has risen above the threshold for a suitable interval. The operation of the power-on reset circuit prevents various integrated circuits such as counters, phase-locked loops, filters, memories, flip-flops, and shift registers, as a few examples, from operating improperly during start-up operation.

In some cases, such as those involving complex logic patterns or unexpected data patterns, an integrated circuit may be determined, incorrectly, to be in a ready state. It may be desirable to only release the circuit when it is in its predetermined state. In some cases, the power-on reset circuits may release logic when the power supply has maintained its threshold level for a predetermined time even though the circuit's logic is not in its predetermined state. Conversely, the power-on reset circuit may

improperly release the integrated circuit because the logic is in the predetermined state even though the power supply level is still ramping.

Thus, there is a need for a system that does not prematurely release an integrated circuit.

Brief Description of the Drawings

Figure 1 is a block diagram of one embodiment of the present invention;

Figure 2 is a block diagram of one embodiment of the present invention;

Figures 3a through 3c are timing diagrams for a plurality of signals in accordance with one hypothetical embodiment;

Figures 4a through 4c are timing diagrams for signals in accordance with another hypothetical embodiment;

Figure 5 is a block diagram for a chip for generating a power-on reset pulse in accordance with one embodiment of the present invention;

Figure 6 is a circuit diagram for one of the blocks shown in Figure 5 in accordance with one embodiment of the present invention; and

Figure 7 is a circuit diagram for additional blocks in the block diagram shown in Figure 5 in accordance with one embodiment of the present invention.